ABSTRACT

A system for validating error detection logic in a system. The system includes a plurality of information paths, each one of such paths having associated therewith an error detection logic, each one of the paths having a plurality of information bits. A test word buffer is provided for receiving a test word, such test word indicating a particular one of the plurality of information bits in a particular one of the information paths to be corrupted. The system includes a plurality of fault injectors responsive to the test word received by the buffer. Each one of the fault injectors is disposed in a corresponding one of the information paths prior to the associated the error detection logic. Each one of such fault injectors corrupts a selected one of the information bits in the corresponding one of the information paths in response to the test word received by the buffer to test whether the associated error detection logic detects such injected fault. The test word buffer stores an indication as to whether software in one of the directors is to be tested for response to a detected fault.